What is claimed is:

1. A method of simulating an application specific processor (ASP) comprising:

defining a functional model in a high level language for simulating the architectural behaviour of the ASP, wherein in the functional model a CPU and a set of peripherals are defined;

generating for each peripheral an interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral in a manner independent of any particular data structure, and a test functions file which defines the communication attributes of the processor with the peripheral in a manner independent of any particular data structure;

simulating in the high level language as part of the functional model an application executable by the CPU and operations of the set of peripherals for a predetermined simulation phase, the application executable by the CPU including the test functions file and the operations of the set of peripherals including the interface functions file;

outputting the state of the application and the state of the peripherals at the end of the predetermined phase to a modelling file in the high level language;

converting the modelling file in the high level language to a simulation language for simulating the ASP at circuit level; and

simulating the ASP at circuit level using the simulation language for a subsequent simulation phase.

2. A simulation method according to claim 1, wherein the functional model in the high level language also simulates environmental stimuli which are also held in the modelling file at the end of the predetermined simulation phase in the high level language.

3. A simulation method according to claim 1, wherein the high level language is C.

4. A simulation method according to claim 1, wherein the simulation language at circuit level is VHDL.

5. A computer system for simulating an application specific processor (ASP) according to the method of claim 1, the computer system comprising:

a first computer for executing the functional model in the high level language and for translating the modelling file into a simulation file at the end of a predetermined phase; and

a second computer for executing the simulation at circuit level using the simulation file.

6. A computer system for simulating an ASP comprising:

first processor means including execution means for simulating a functional model in a high level language and output means for outputting the state of the functional model at the end of a predetermined simulation phase;

means for converting the functional model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at circuit level; and

second processor means arranged to execute the simulation language to simulate the ASP at circuit level for a subsequent simulation phase.

7. A modelling file stored on a computer readable medium and comprising a first code portion holding a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test function file after a predetermined simulation phase and a second code portion holding an interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after a predetermined simulation, wherein the code portions are within a circuit level simulation language and are executable by a computer in which the modelling file is loaded to simulate the ASP at circuit level for a subsequent simulation phase.